Abstract of the Disclosure:

A decoding apparatus includes at least one decoder both for a turbo-decoding and for a Viterbi decoding, at least one first data path for the Viterbi decoding of a convolution code, at least one second data path for the decoding of a turbo code, and a common memory having a multiplicity of individual memory areas. It is possible to allocate at least one memory area both through the first data path in the Viterbi mode and through the second data path in the turbo mode. The invention also includes a trellis processor and a method for operating a decoding apparatus in which at least parts of the first data path and of the second data path can be utilized jointly both for the turbo decoding and for the Viterbi decoding.

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